EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	14	clock adj generators near5 circuit near5 first near2 second	USPAT	OR	OFF	2007/02/22 17:55
S2	3	clock adj generators near5 circuit near5 first near2 second	US-PGPUB	OR	OFF	2007/02/22 17:57
S3	0	clock adj generators near5 circuit near5 first near2 second	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:00
S4	3	first adj circuit with second adj circuit with normal with standby	USPAT	OR	OFF	2007/02/22 18:01
S5	2	first adj circuit with second adj circuit with normal with standby	US-PGPUB	OR	OFF	2007/02/22 18:05
S6	0	first adj circuit with second adj circuit with normal with standby	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:05
S7	63	copy$3 with first adj register with second adj register	USPAT	OR	OFF	2007/02/22 18:12
S8	0	copy$3 with first adj register with second adj register with (standby normal wak$3)	USPAT	OR	OFF	2007/02/22 18:13
S9	1	copy$3 with first adj register with second adj register same (standby normal wak$3)	USPAT	OR	OFF	2007/02/22 18:13
S10	2	copy$3 with first adj register with second adj register same (standby normal wak$3)	US-PGPUB	OR	OFF	2007/02/22 18:13
S11	0	copy$3 with first adj register with second adj register same (standby normal wak$3)	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:13
S12	1	(first adj circuit) near3 standby with (second adj circuit) near3 (normal wak$3)	USPAT	OR	OFF	2007/02/22 18:15
S13	1	(first adj circuit) near3 standby with (second adj circuit) near3 (normal wak$3)	US-PGPUB	OR	OFF	2007/02/22 18:15
S14	0	(first adj circuit) near3 standby with (second adj circuit) near3 (normal wak$3)	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:16
S15	182	first adj register with first adj clock	USPAT	OR	OFF	2007/02/22 18:16
S16	77	first adj register with first adj clock same second adj register with second adj clock	USPAT	OR	OFF	2007/02/22 18:17
S17	0	first adj register with first adj clock same second adj register with second adj clock same standby	USPAT	OR	OFF	2007/02/22 18:17

EAST Search History

S18	0	first adj register with first adj clock same second adj register with second adj clock same copy$3	USPAT	OR	OFF	2007/02/22 18:17
S19	1	first adj register with first adj clock same second adj register with second adj clock same normal	USPAT	OR	OFF	2007/02/22 18:18
S20	2	first adj register with first adj clock same second adj register with second adj clock same normal	US-PGPUB	OR	OFF	2007/02/22 18:18
S21	0	first adj register with first adj clock same second adj register with second adj clock same normal	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:19
S22	11	event with shadow adj register	USPAT	OR	OFF	2007/02/22 18:19
S23	11	event with shadow adj register	US-PGPUB	OR	OFF	2007/02/22 18:21
S24	1	event with shadow adj register	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:21
S25	0	control$3 near2 power near5 (first adj circuit near3 second adj circuit)	USPAT	OR	OFF	2007/02/22 18:23
S26	399	control$3 near2 power near5 first adj circuit	USPAT	OR	OFF	2007/02/22 18:23
S27	15	control$3 near2 power near5 first adj circuit with second adj circuit	USPAT	OR	OFF	2007/02/22 18:24
S28	10	control$3 near2 power near5 first adj circuit with second adj circuit	US-PGPUB	OR	OFF	2007/02/22 18:25
S29	0	control$3 near2 power near5 first adj circuit with second adj circuit	EPO; JPO; IBM_TDB	OR	OFF	2007/02/22 18:26
S30	21	ueda.in. with tomohiro	USPAT	OR	OFF	2007/02/22 18:42
S31	818	713/323.ccls.	USPAT	OR	OFF	2007/02/26 11:01
S32	0	713/323.ccls. and first adj circuit with second adj circuit with normal with standby	USPAT	OR	OFF	2007/02/26 11:09
S33	0	713/323.ccls. and copy$3 with first adj register with second adj register same (standby normal wak$3)	USPAT	OR	OFF	2007/02/26 11:09
S34	0	713/323.ccls. and (first adj circuit) near3 standby with (second adj circuit) near3 (normal wak$3)	USPAT	OR	OFF	2007/02/26 11:10
S35	0	713/323.ccls. and event with shadow adj register	USPAT	OR	OFF	2007/02/26 11:11
S36	1	713/323.ccls. and control$3 near2 power near5 first adj circuit with second adj circuit	USPAT	OR	OFF	2007/02/26 11:12
S37	750	713/324.ccls.	USPAT	OR	OFF	2007/02/26 11:12

EAST Search History

S38	0	713/324.ccls. and (first adj circuit) near3 standby with (second adj circuit) near3 (normal wak$3)	USPAT	OR	OFF	2007/02/26 11:18
S39	0	713/324.ccls. and event with shadow adj register	USPAT	OR	OFF	2007/02/26 11:18
S40	0	713/324.ccls. and copy$3 with first adj register with second adj register same (standby normal wak$3)	USPAT	OR	OFF	2007/02/26 11:19
S41	1	713/324.ccls. and control$3 near2 power near5 first adj circuit with second adj circuit	USPAT	OR	OFF	2007/02/26 11:19
S42	1	713/324.ccls. and first adj circuit with second adj circuit with normal with standby	USPAT	OR	OFF	2007/02/26 11:20
S43	519	365/229.ccls.	USPAT	OR	OFF	2007/02/26 11:21
S44	0	365/229.ccls. and (first adj circuit) near3 standby with (second adj circuit) near3 (normal wak$3)	USPAT	OR	OFF	2007/02/26 11:25
S45	0	365/229.ccls. and event with shadow adj register	USPAT	OR	OFF	2007/02/26 11:26
S46	0	365/229.ccls. and copy$3 with first adj register with second adj register same (standby normal wak$3)	USPAT	OR	OFF	2007/02/26 11:26
S47	1	365/229.ccls. and control$3 near2 power near5 first adj circuit with second adj circuit	USPAT	OR	OFF	2007/02/26 11:27
S48	0	365/229.ccls. and first adj circuit with second adj circuit with normal with standby	USPAT	OR	OFF	2007/02/26 11:27